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Design and Implementation of 16-bit Arithmetic Logic Unit using Quantum dot Cellular Automata (QCA) Technique

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Abstract —
Quantum Dot Cellular Automata (QCA) is an advanced nanotechnology that attempts to create general computational at the nano-scale by controlling the position of single electrons. Quantum dot cellular automata (QCA) defines a new device architecture that permits the innovative design of digital systems. QCA technology has large potential in terms of high space density and power dissipation with the development of the faster computer with smaller size & low power consumption.QCA help us to overcome the limitations of CMOS technology. In this paper, A design 16-bit arithmetic logic unit (ALU) based on the Quantum dot cellular automata (QCA) is presented.
The simulation result of 16 bit ALU is verified using QCA Designer tool.
Index Terms – ALU, Quantum Dot Cellular Automata (QCA), nano Technology.

I. INTRODUCTION

There has been extensive research in recent years at nano scale to supersede conventional CMOS technology. Over the last few decades, the exponential scaling in feature sizes & the increase in processing power have been successfully achieved by conventional lithography based very large scale integration (VLSI) technology. Quantum-dot Cellular Automata provides new possibilities for computing owing to its unique properties .QCA has significant advantages of fast speed, high density & low power consumption. QCA relies on afresh physical phenomena (coulombic interaction) and its logic states are not stored as voltage levels, but rather the position of individual electronics. the QCA is a new technology which not only gives a solution to realize nano ICs but also lays a platform for computation & information exchange at nano scale.
This paper presents the design & layout of an 16-bit arithmetic logic unit using QCA Designer tool.

II. Overview of QCA

A.QCA cell

QCA is based upon the encoding of binary information in the charge configuration within quantum dot cells. A fundamental QCA is made up of four quantum dots which are located on vertices of a square, also there are two electrons in a QCA cell that can tunnel between dots inside the cell. The electrons must be located on the opposite corners of square according to the coulomb repulsion in grounds state. Two bi stable states result in polarizations of p = +1 & p= -1 as shown in fig.

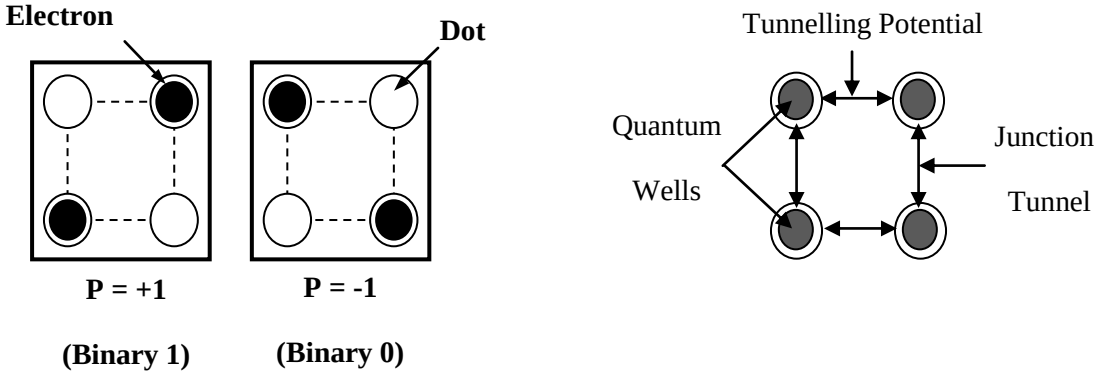


Fig.1: QCA cell & 4-dot QCA cell with its possible polarization

B. QCA Majority gate-

QCA majority gate (MG) consists of 4 QCA cells around a centre QCA cell. It performs a logic, a logic function M (A,B,C) on three inputs say A, B, C as

M (A,B,C) = A.B +B.C+A.C

Gates such as AND & OR can be realized by forcing a single input to -1 & +1 respectively

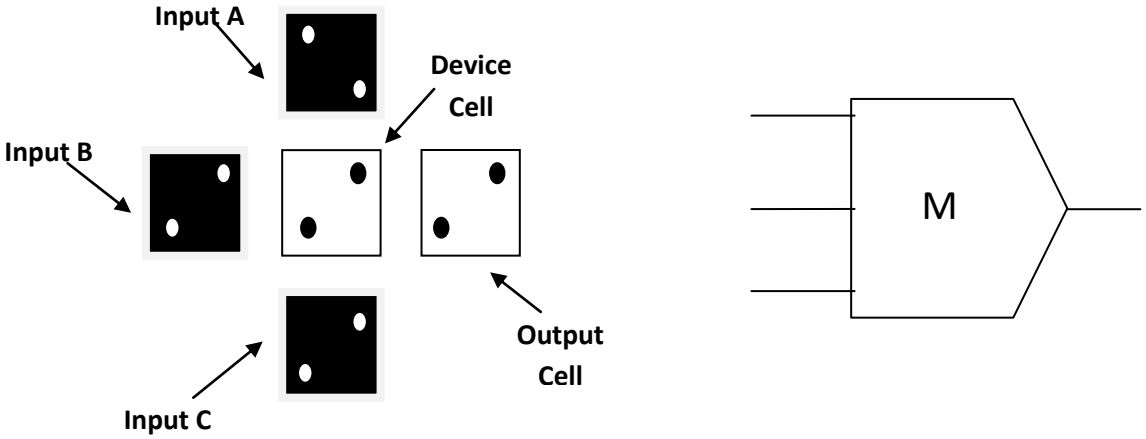


Fig2: majority gate (MG) with symbol

C. QCA Clocking –

Timing in QCA is accomplished by a cascaded clocking of four distinct & periodic phases. The four clock phases shown fig.4 are used as switch, hold release & relaxed. In the first (switch) phase, the tunneling barrier between two dots start to rise. The second (hold) phase is reached when the tunneling. In third (release) phase Barrier falls from high to low the final phase (relax) ensures there is no inter dot barrier & the cell remains un-polarized.

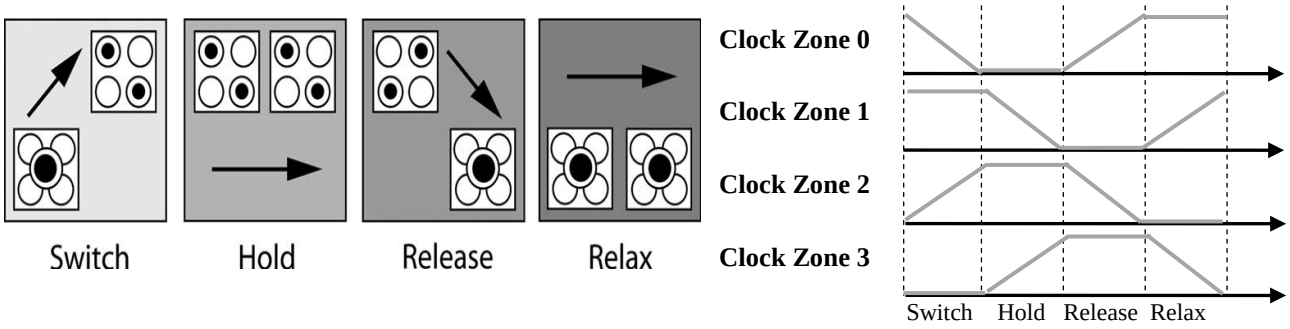


Fig 3: clocking zones in QCA

III. ARCHITECTURE OF 16 BIT ALU-

An arithmetic logic unit is a multi operation, Combinational –logic digital function.

It can Perform a set of basic arithmetic operations and a set of logic operation. The ALU has a number of selection lines to select a particular operation in the unit. The ALU has three selection lines to select a particular operation in the unit M is master select line the operation either arithmetic or logical & S0 and S1 are other select lines to select various operations.

The arithmetic logic unit consist three basics units, arithmetic, logical unit & ripple carry adder circuit. Block diagram of 16-bit ALU shown in fig.6.

A. ARITHMETIC UNIT-

The arithmetic unit is designed to perform four operations. Addition, subtraction, increment & decrement. The function table, truth table & logic diagram are described. Initial carry is C0 is given by equation below is given, where

$$C_0 = MS_1 \qquad \text{… (1)}$$

Table1: Functional Table & truth table of arithmetic unit-

According to truth table we write Boolean equation of arithmetic unit shown in equation (2) and design logic circuit of arithmetic unit shown in fig. 4.

$$Y = M\overline{S_1}B + M\overline{S_0}\overline{B} \qquad \text{… (2)}$$

M	S_1	S_0	Function name	Function	X	Y	C_0
1	0	0	Decrement	A-1	A	all 1's	0
1	0	1	Add	A+B	A	B	0
1	1	0	Subtract	A+B'+1	A	B'	1
1	1	1	Increment	A+1	A	all 0's	1

M	S_1	S_0	B	Y
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	1	0	0
1	1	1	0	0
1	1	1	1	0

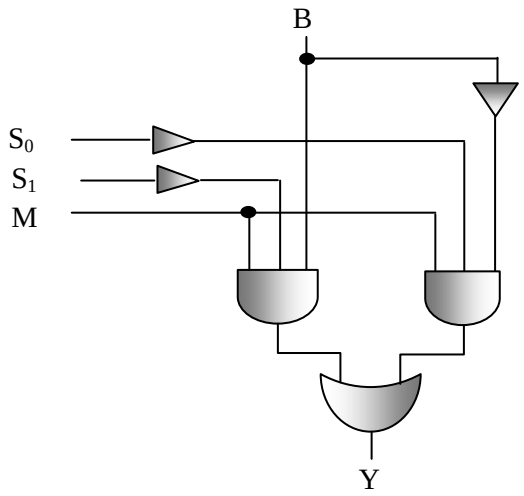


Fig. 4: Logic diagram of arithmetic unit

B. LOGICAL UNIT –

The logic operations are performed in logic unit. The logic unit can perform four operations based on the select input S0 & S1. These are Complement, AND, OR and Identity.

Table3: Functional Table & truth table of Logical Unit-

M	S_1	S_0	Function	Function	X	Y	C_0
0	0	0	Complement	A’	A’	0	0
0	0	1	AND	A and B	A&B	0	0
0	1	0	Identity	A	A	0	0
0	1	1	OR	A or B	A|B	0	0

M	S_1	S_0	X
0	0	0	A’
0	0	1	A & B
0	1	0	A
0	1	1	A | B
1	X	X	A

According to truth table we write Boolean equation of logical unit shown in equation (3) and design logic circuit of logical unit shown in fig. 5.

$$\boldsymbol{X = \bar{M}\overline{S_1 S_0}\bar{A} + \bar{M}S_1 S_0 B + S_0 AB + S_1 A + MA} \quad \textbf{… (3)}$$

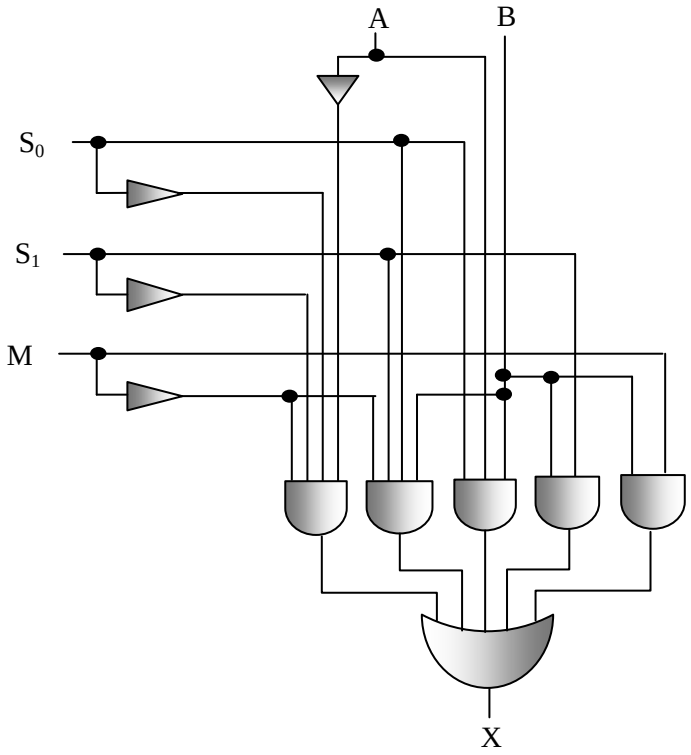


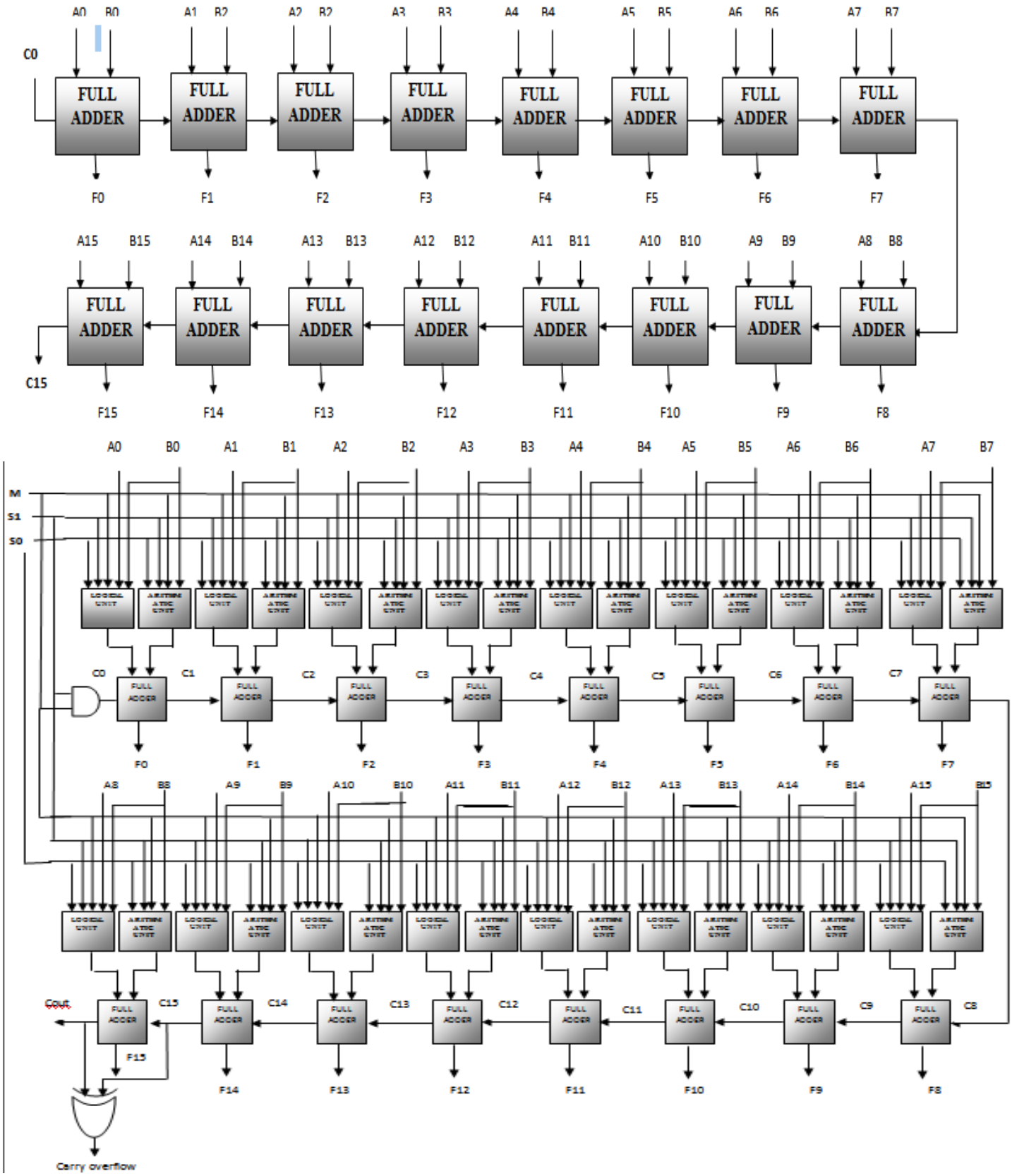
Fig. 5: Logic diagram of logical unit

A.RIPPLE CARRY ADDER –

Adders are usually implemented by combining multiple copies of simple components. The natural components for addition are half adders or full adders. The principal problem in constructing an adder for n-bit numbers out of small pieces is propagating carries from one piece to the next.

The most obvious way to solve this with a ripple carry adder, consisting of n full adders, illustrated in Figure 6, where each block consists of full adder. The carry out of one full adder is connected to the carry in of the adder for the next most significant bit. The carries ripple from the least significant bit (on the right) to the most significant bit. In general, the time a circuit takes to produce an output is proportional to the maximum number of logic levels through which a signal travels. It takes two levels for first carry to compute from A_0 and B_0.The ripple carry adders are slowest but also the cheapest. It can be built with only n simple cells, connected in a simple, regular way.

Fig6: 16-bit ripple carry adder & architecture of 16-bit ALU shown in below -



IV.IMPLEMENTATION OF 16-BIT ALU IN QCA –

Implementation of 16-bit Arithmetic Logic Unit in QCA is verified using QCA Designer tool. The inputs are at the top side and the outputs are at the bottom side in QCA layout of ALU. The proposed design is shown in Figure 7.

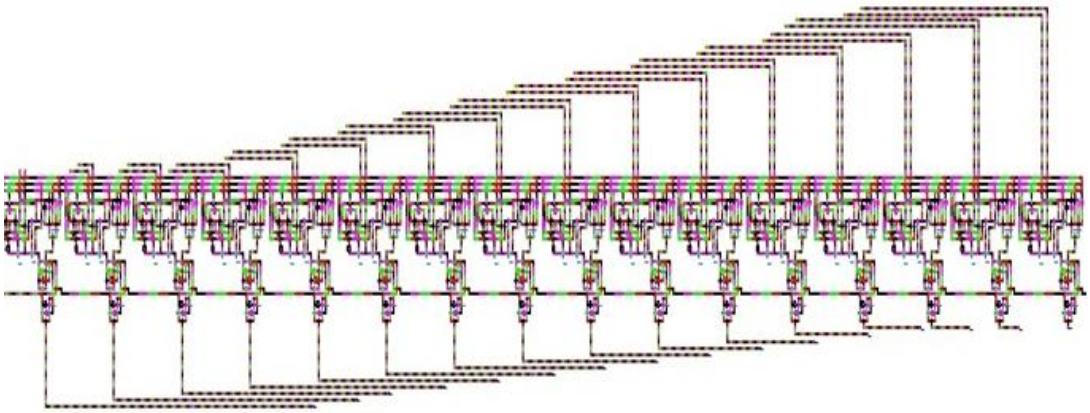


Figure 7: implementation of 16-bit ALU in QCA

V.SIMULATION RESULTS AND DISCUSSION–

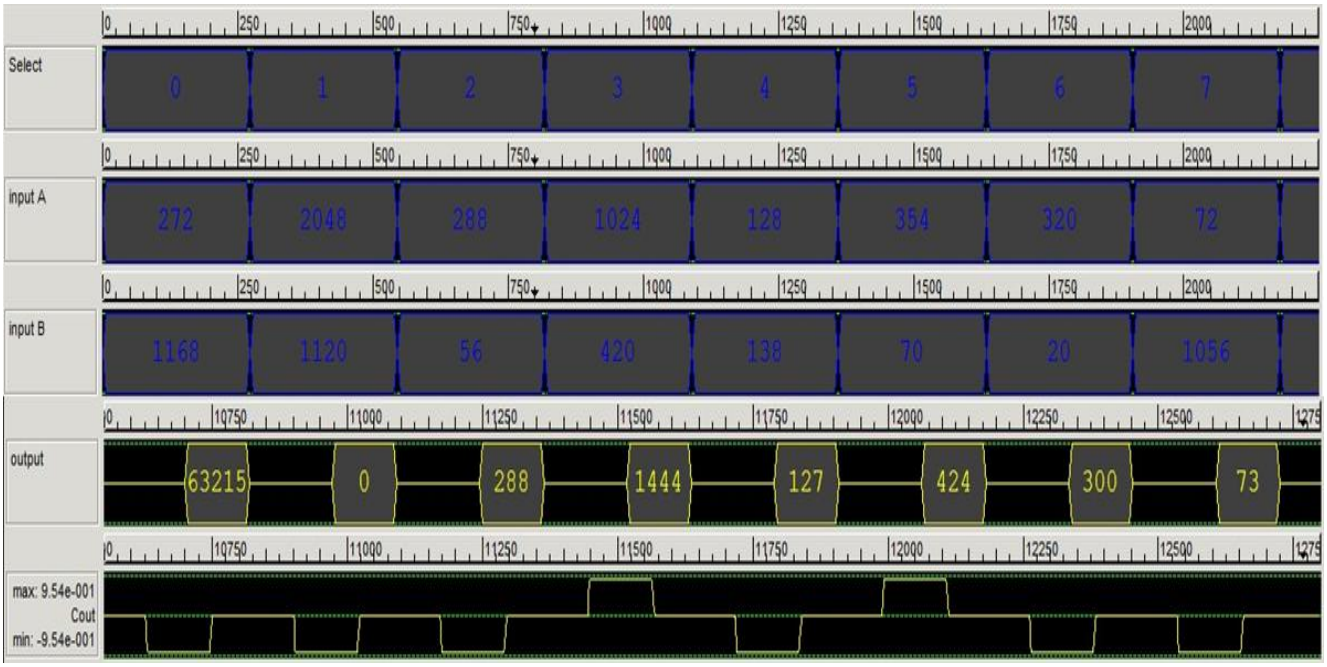


Figure 8: simulation result of 16 bit ALU in QCA

All the designs were verified using QCADesigner tool ver. 2.0.3. In the bi-stable approximation, we used the following parameters: cell size=18 nm, number of samples=12800, convergence tolerance=0.001000, radius of effect=65.00 nm, relative permittivity=12.900000The simulation Results of 16-bit ALU is shown in figure 8. According to simulation results, as we seen the highlighted area is the output of ALU and the QCA circuit of 16-bit ALU has delay of 39 clocks. This result shows the outputs are same as function table of ALU .

VI . CONCLUSION-

This paper presents the design of 16-bit Arithmetic Logic Unit based on Quantum-dot Cellular Automata, which uses multilayer crossovers. Presented design construct using arithmetic, logical and ripple carry adder which have minimum complexity (23021 cells), smaller size of 70.60μm^2 and cheap in cost because of its size. The proposed design of 16-bit ALU is much more beneficial.

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